

Fig. 1

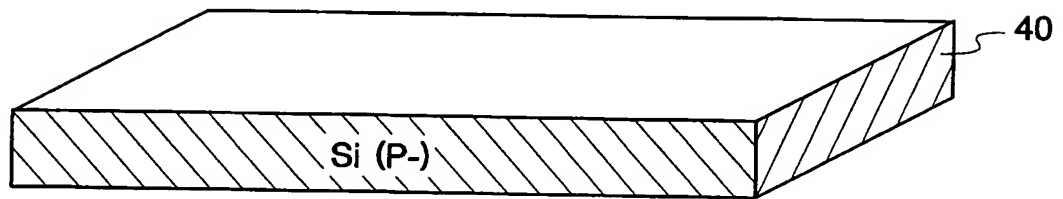


Fig. 2

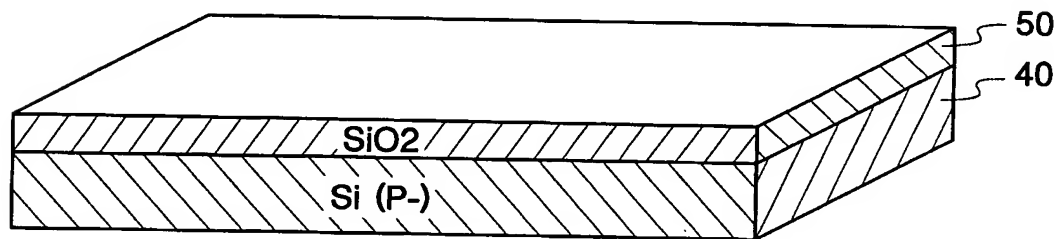


Fig. 3

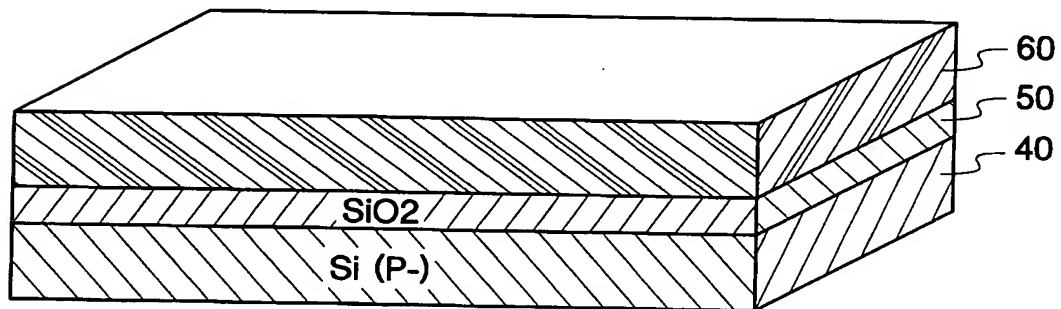


Fig. 4

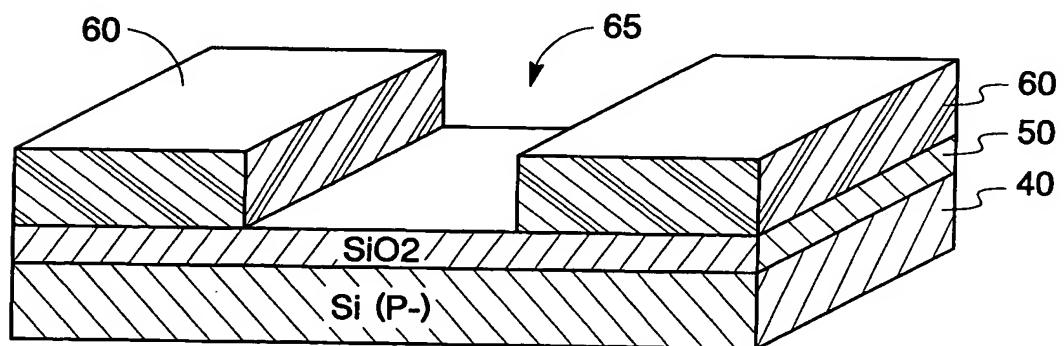


Fig. 5

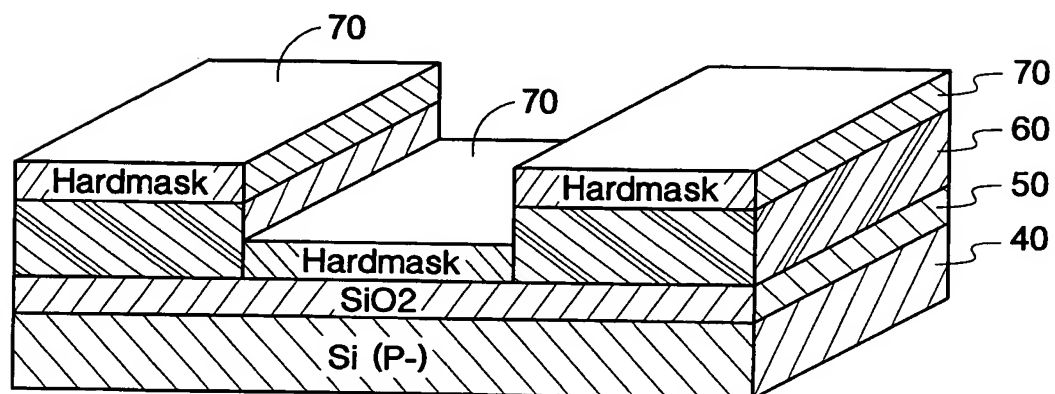


Fig. 6

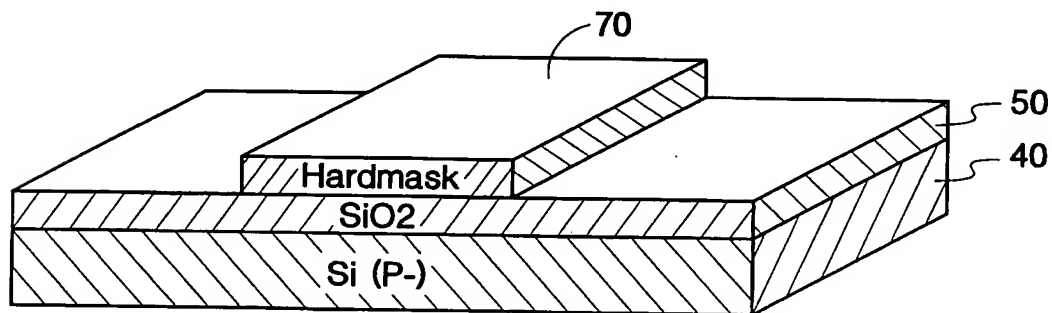


Fig. 7

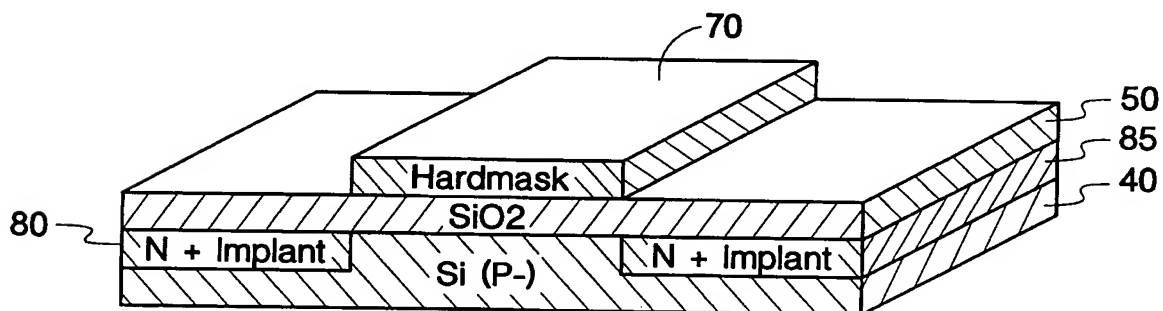


Fig. 8

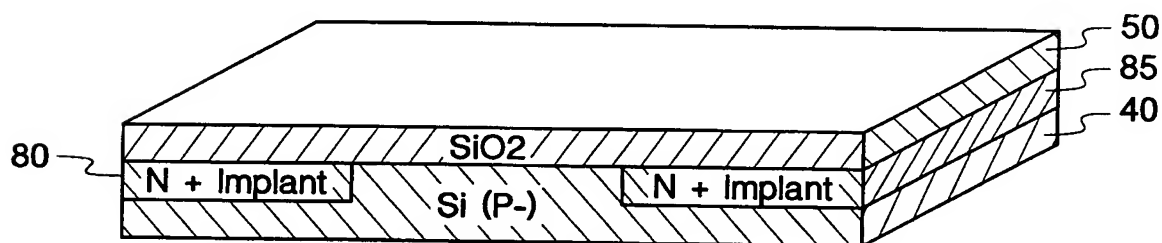


Fig. 9

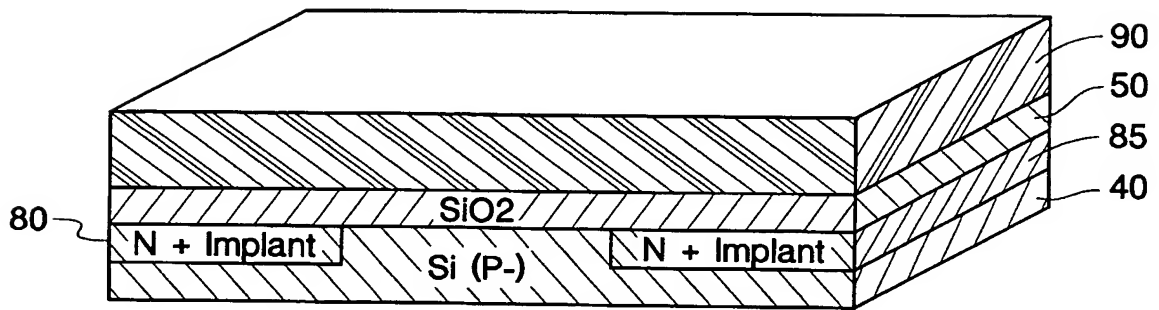


Fig. 10

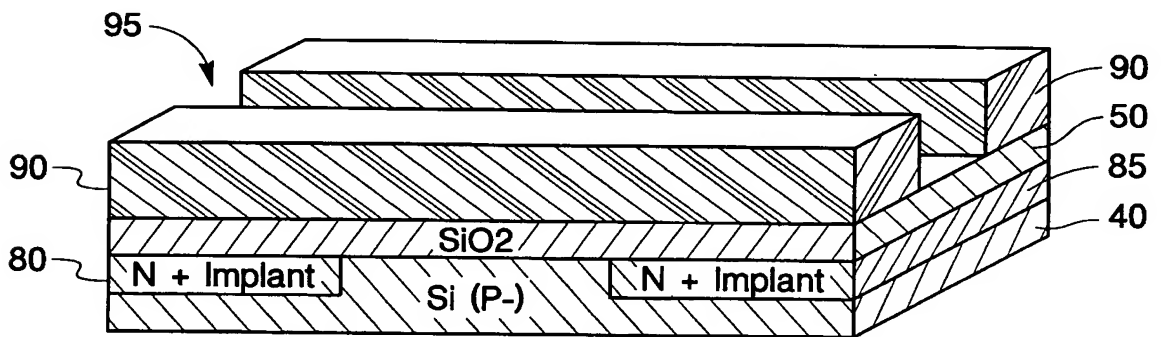


Fig. 11

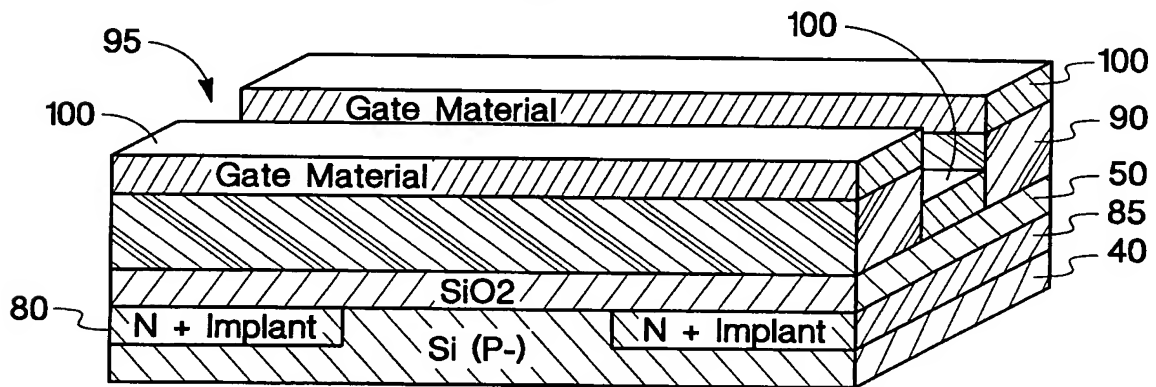


Fig. 12

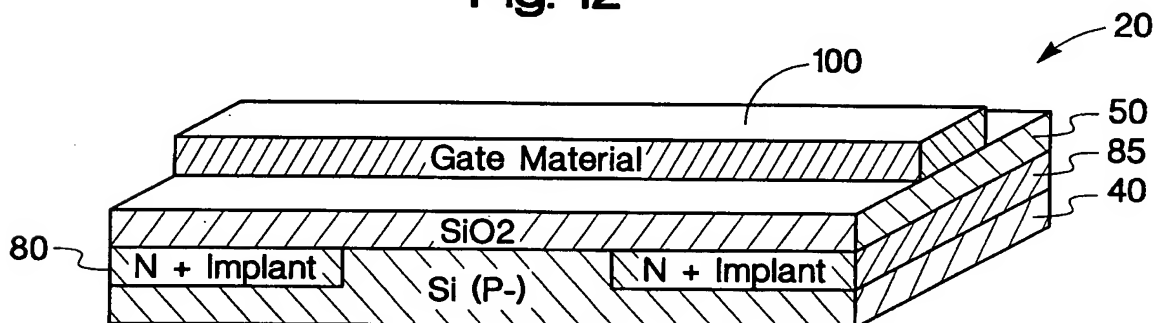


Fig. 13

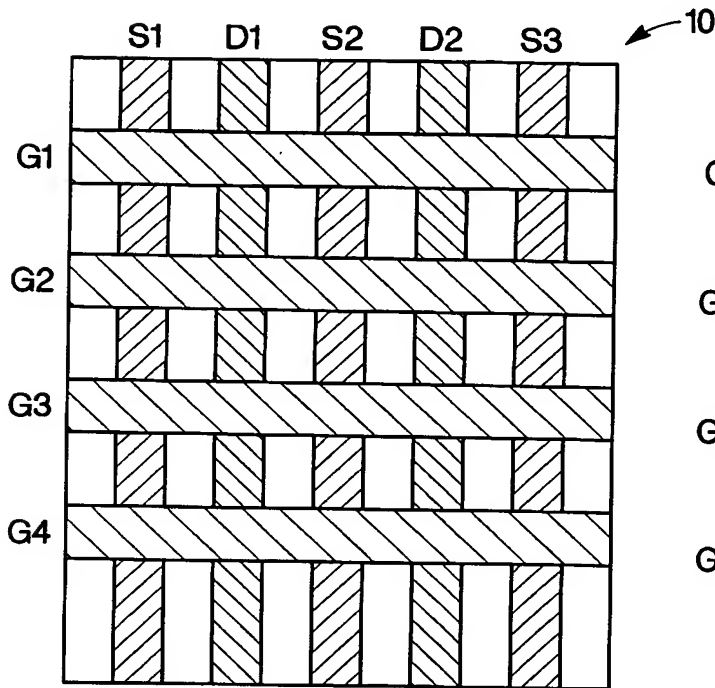


Fig. 14a

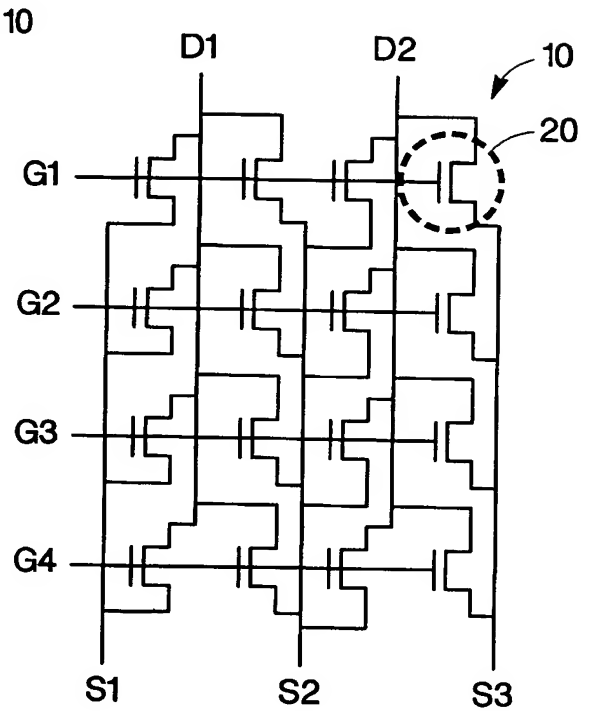


Fig. 14b

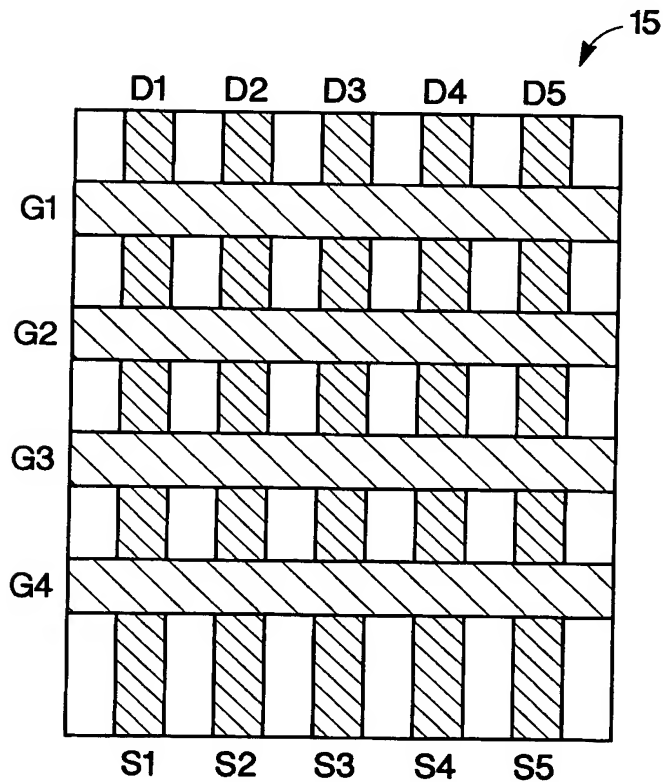


Fig. 15a

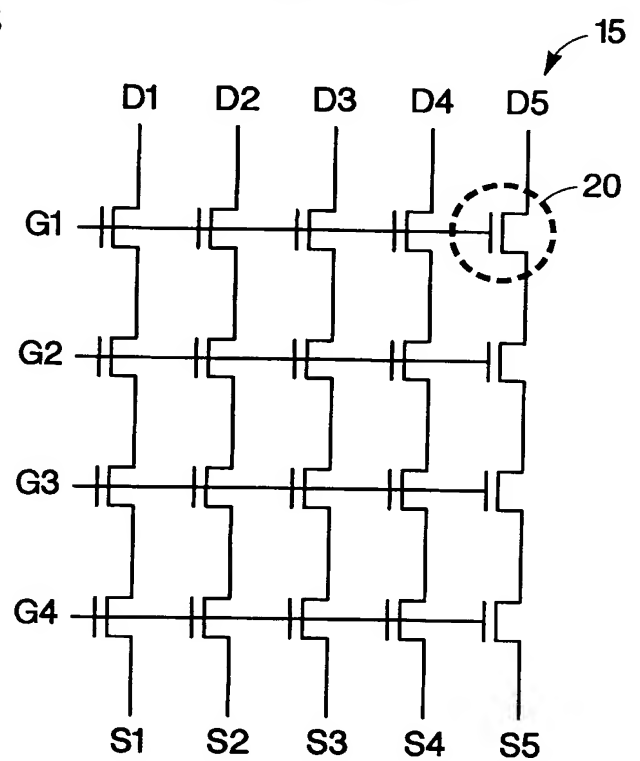


Fig. 15b

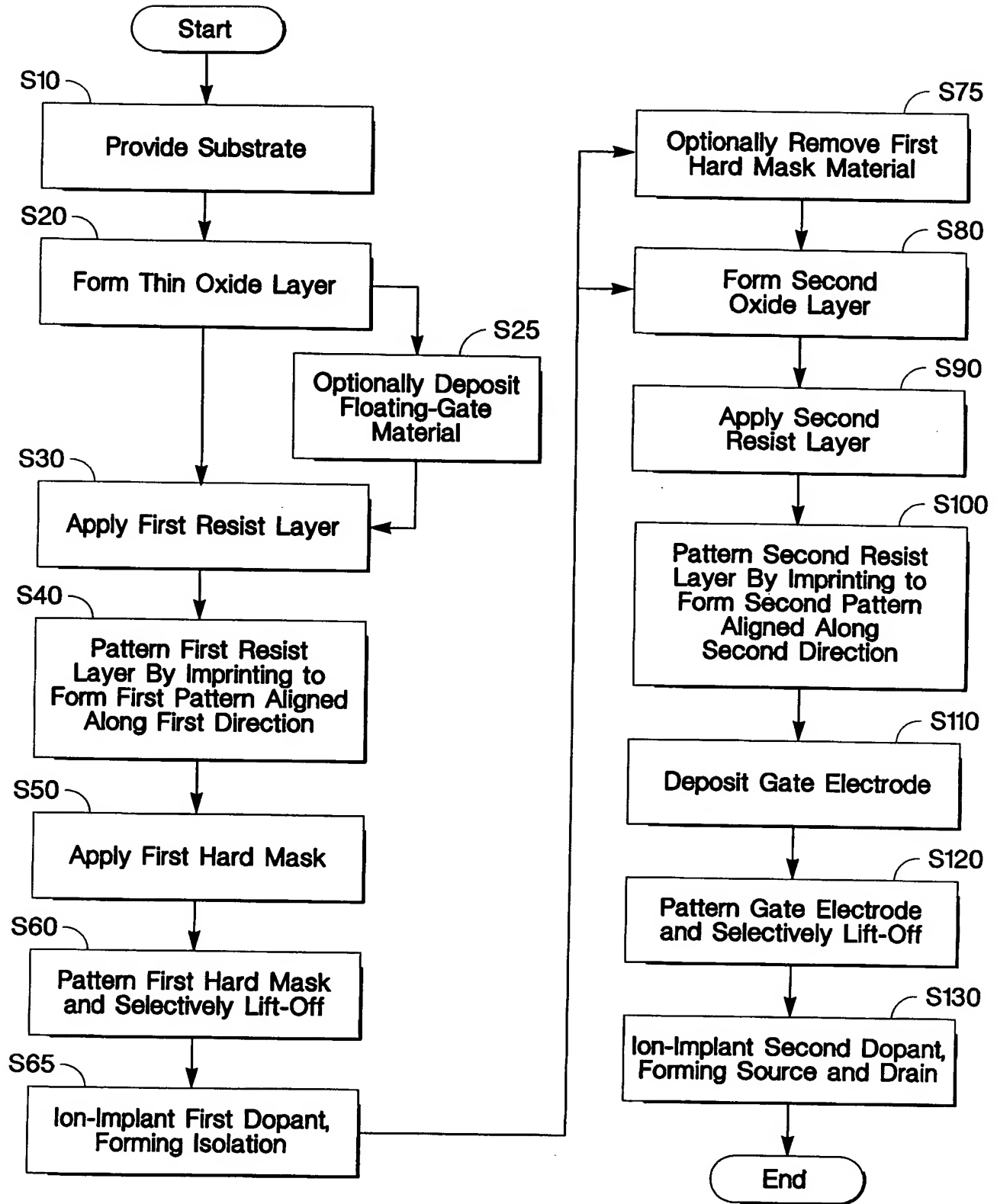


Fig. 16

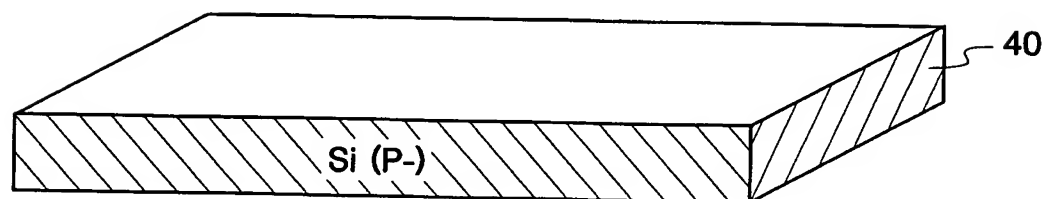


Fig. 17

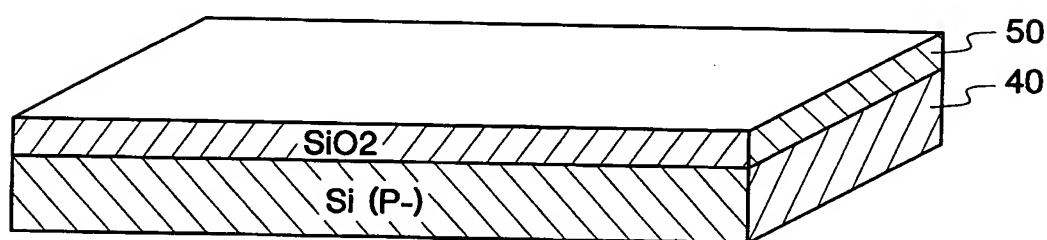


Fig. 18

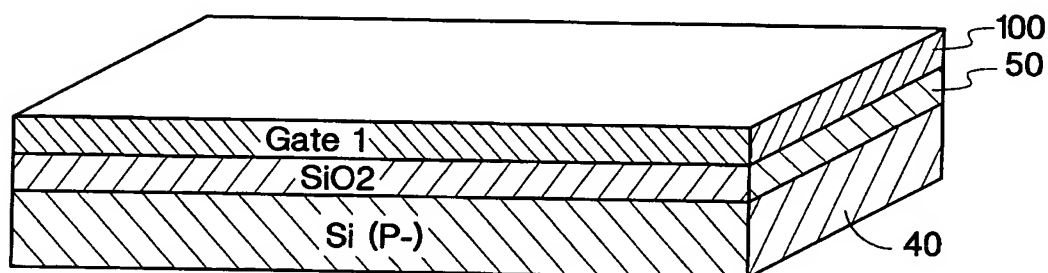


Fig. 19

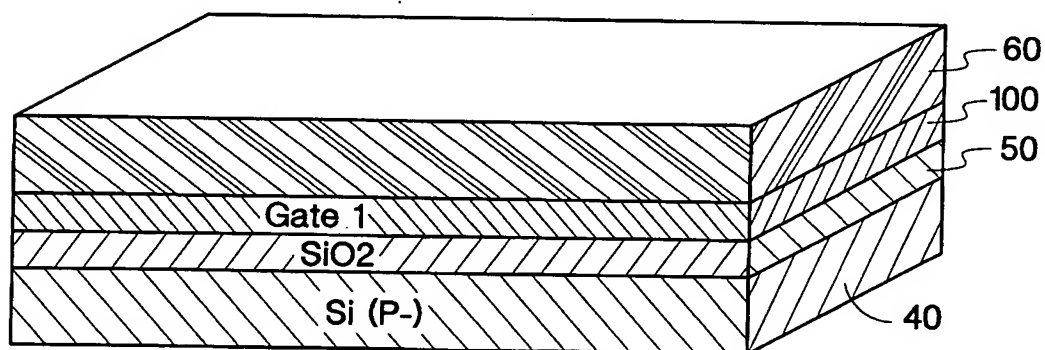


Fig. 20

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A cross-sectional view of a semiconductor device. The substrate is labeled 40 and consists of a Si (P-) layer and a SiO₂ layer. A gate structure, labeled Gate 1, is formed on the SiO₂ layer. The gate structure includes a gate dielectric layer 60 and a gate electrode layer 65. The gate electrode layer 65 is divided into two regions, 60 and 65, by a gap. The gate dielectric layer 60 is divided into three regions, 60, 100, and 50, by the gap. The gate electrode layer 65 is divided into two regions, 60 and 65, by the gap. The gate dielectric layer 60 is divided into three regions, 60, 100, and 50, by the gap. The gate electrode layer 65 is divided into two regions, 60 and 65, by the gap.

This diagram shows a cross-sectional view of a semiconductor device after the first gate formation step. The substrate is labeled 40 and consists of a Si (P-) layer, a SiO₂ layer, and a Gate 1 layer. The Gate 1 layer is a thin layer of material, possibly polysilicon, that has been deposited and then patterned. The SiO₂ layer is a thin layer of silicon dioxide that has been deposited over the Gate 1 layer. The Si (P-) layer is the substrate material, which is p-type silicon. The device is shown with a central gate region and two side regions. The side regions are labeled 60 and 70. The central gate region is labeled 70. The side regions 60 and 70 are the regions where the gate material has been removed, leaving the SiO₂ layer exposed. The central gate region 70 is the region where the gate material has been deposited, forming a thin layer over the SiO₂ layer. The side regions 60 and 70 are the regions where the gate material has been removed, leaving the SiO₂ layer exposed. The central gate region 70 is the region where the gate material has been deposited, forming a thin layer over the SiO₂ layer. The side regions 60 and 70 are the regions where the gate material has been removed, leaving the SiO₂ layer exposed.

Fig. 24

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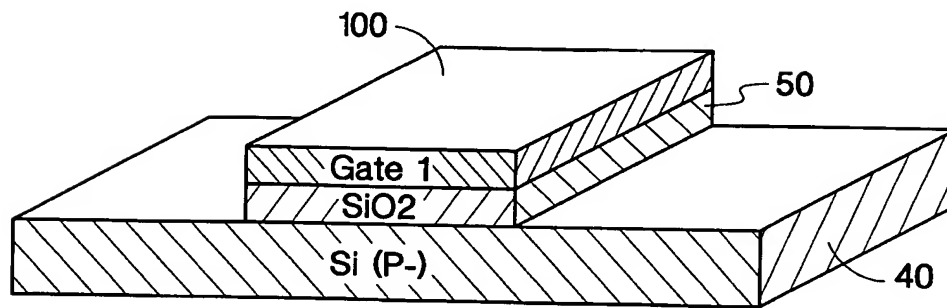


Fig. 25

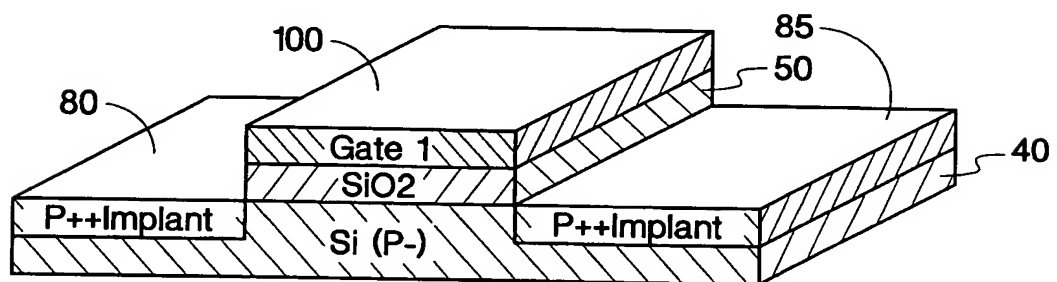


Fig. 26

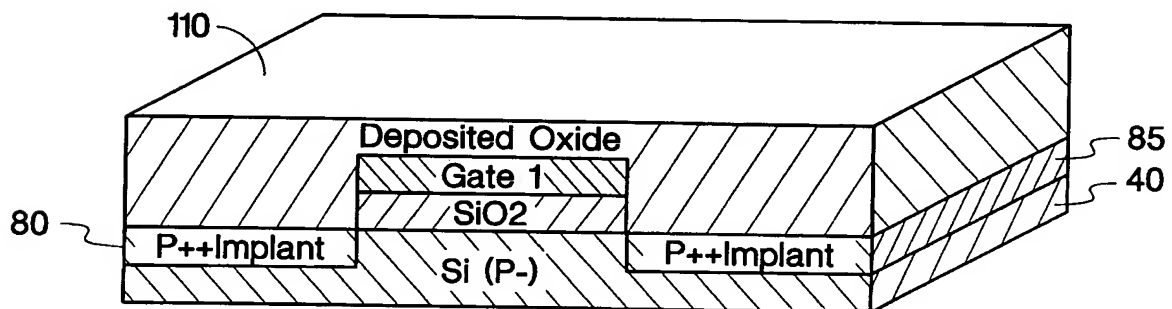


Fig. 27

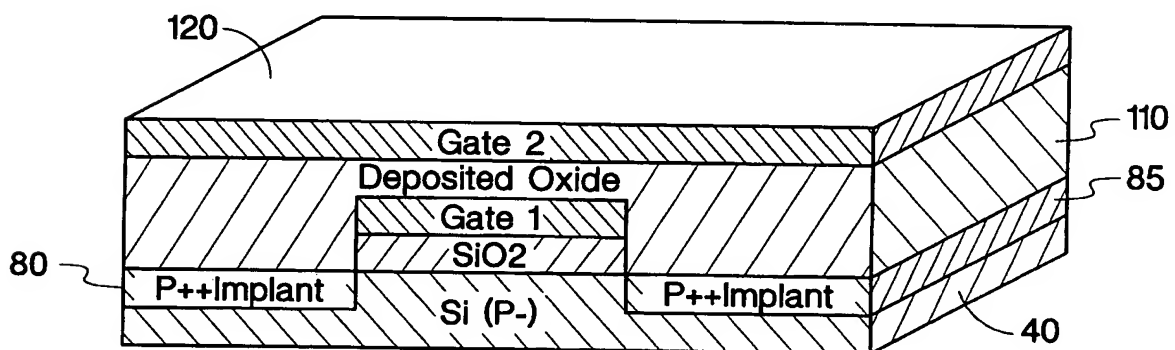


Fig. 28

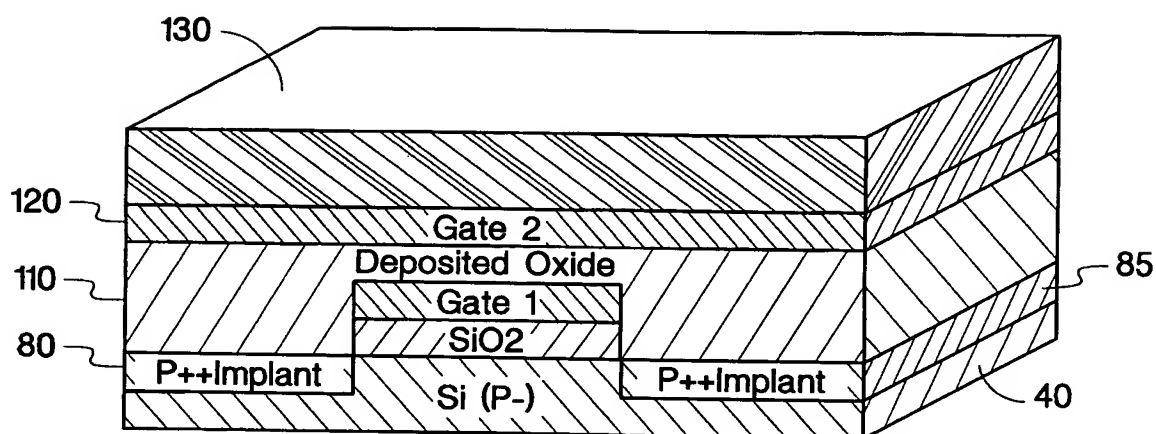


Fig. 29

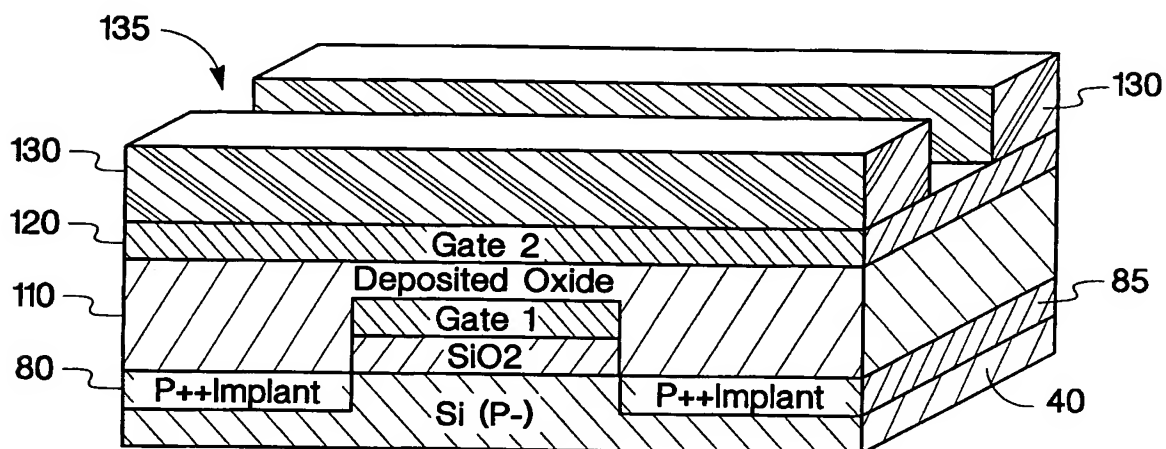


Fig. 30

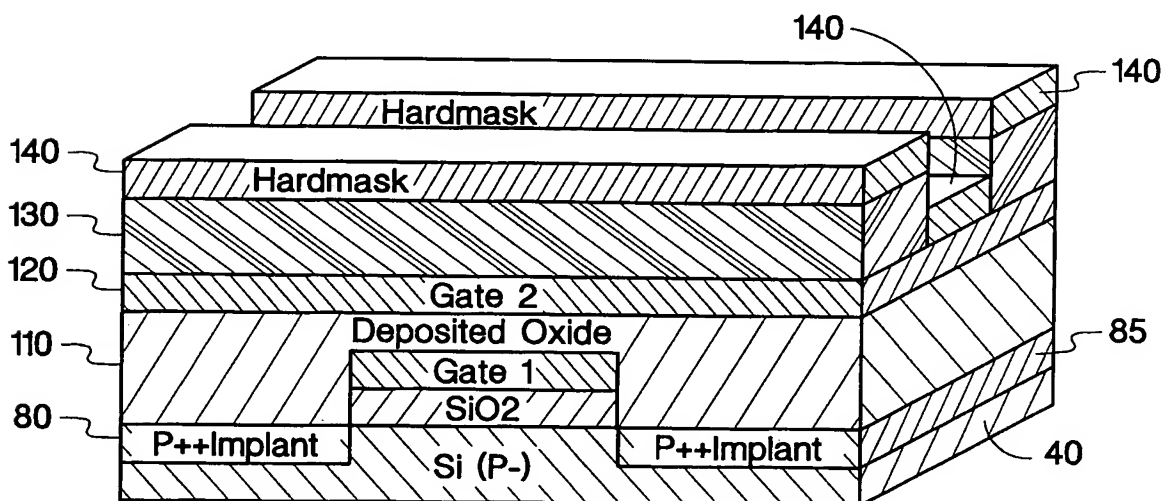


Fig. 31

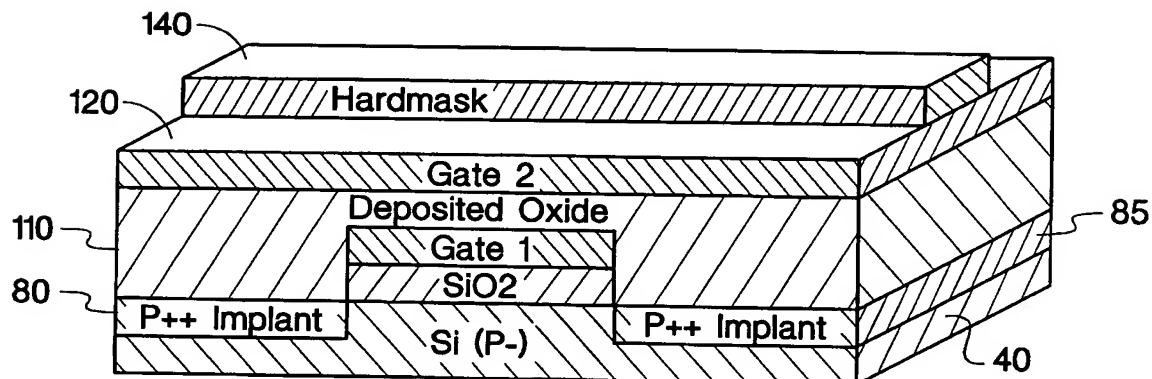


Fig. 32

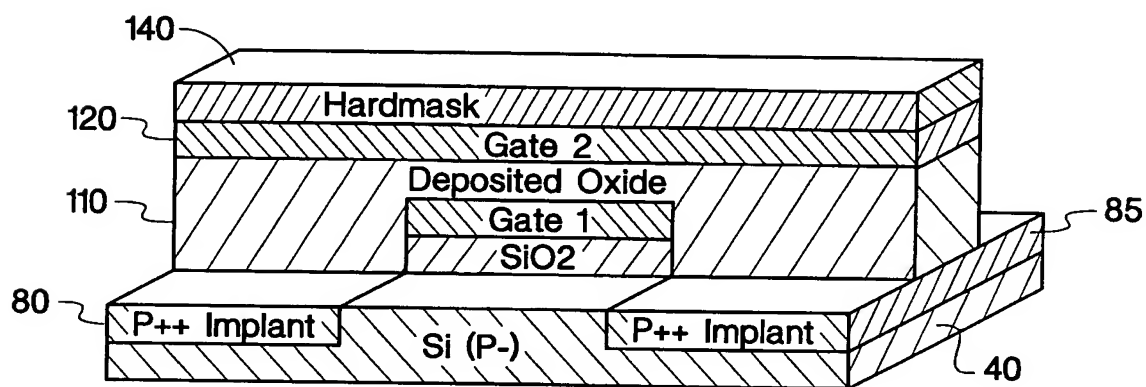


Fig. 33

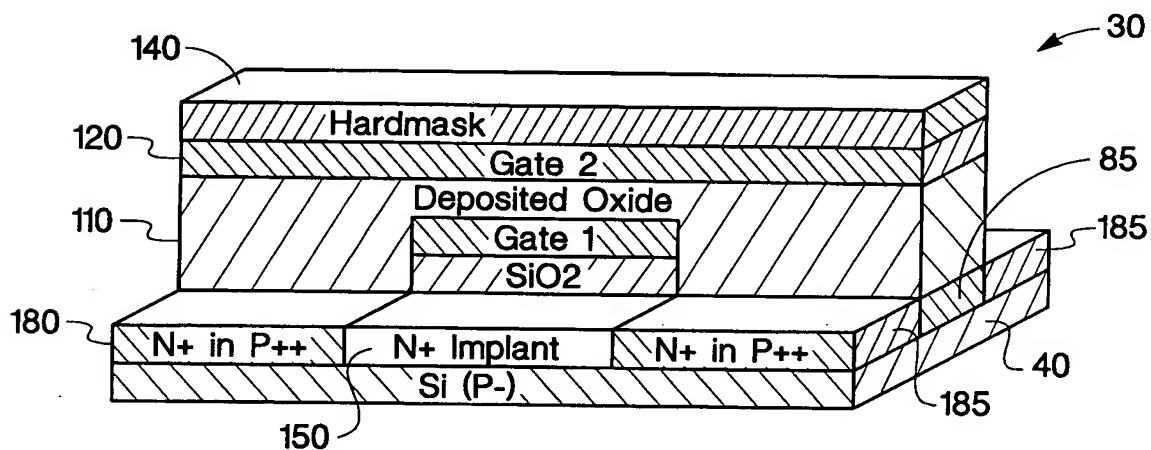


Fig. 34